Call for Papers

ACM JETC Special Issue on

Hardware and Algorithms for Learning On-a-chip

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Machine learning algorithms have made significant progress in recent years, achieving accuracy close to, or even better than human-level perception in various tasks, such as image based search, multi-category classification, and scene analysis. However, most of the approaches heavily rely on the availability of large datasets and the time-consuming off-line training to generate an accurate model, which are major limitations in applications with dynamic variations and personalized needs. In addition, the computational complexity of deep learning and computer vision algorithms still challenges the state-of-the-art computing platforms, especially when the application of interest is tightly constrained by the requirements of low power, high throughput, small latency, etc.

In recent years, there have been enormous advances in implementing machine learning algorithms with application-specific hardware (e.g., FPGA, ASIC, etc.). There is a timely need to map the latest learning algorithms to physical hardware, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness. Recent progress in computational neurosciences and nanoelectronic technology, such as resistive memory devices, will further help shed light on future hardware-software platforms for learning on-a-chip.

In this context, a holistic approach of concurrent innovations in hardware and algorithms is essential to support real-time information analytics under stringent power constraints in a mobile system. The overarching goal of this special issue is to explore the potential of on-chip machine learning, to reveal emerging algorithms and design needs, and to promote novel applications for learning.

The key topics of interest include, but are not limited to the following:

- Hardware acceleration for machine learning
- Deep learning with high speed and high power efficiency
- Hierarchical learning and classification on a chip
- Hardware implementation of sparse coding, feature extraction and personalization
- Hardware and computation models of the cortical and sensory systems
- Nanoelectronic devices, circuits and architectures for neuromorphic computing
- Emerging applications of on-chip learning, including mobile computing, automotive vision, etc.

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- Author Notification: June 1, 2016
- Revised Manuscript Due: July 15, 2016
- Notification of Acceptance: September 15, 2016
- Final Manuscript Due: October 30, 2016
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