



Call for Papers

ACM JETC Special Issue on

Hardware and Algorithms for Energy-Constrained On-chip Machine Learning

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Recently, machine/deep learning algorithms has unprecedentedly improved the accuracies in practical recognition and classification tasks. However, to achieve incremental accuracy improvement, state-of-the-art deep neural network (DNN) algorithms tend to present very deep and large models, which poses significant challenges for custom hardware implementations in terms of computation, memory, and communication. This is especially true for energy-/resource-constrained hardware platforms (e.g. mobile/wearable devices, self-driving cars, IoT systems, etc.), where various constraints exist in power, performance, and area.

There is a timely need to map the latest machine learning algorithms to application-specific hardware (e.g., ASIC, FPGA, emerging devices, etc.), in order to achieve orders of magnitude improvement in performance, energy efficiency and density. Recent progress in emerging hardware-friendly algorithms and nanoelectronic technology will further help shed light on future hardware-software platforms for on-chip learning. In 2015, 2016 and 2017, the workshops on Hardware and Algorithms for Learning On-a-chip (HALO) were successfully organized, resulting in two special issues in JETC in 2016 and 2018. To address the rapid progress in this field, this new special issue is proposed to report energy-efficient on-chip machine learning algorithm and hardware designs.

The objective of this special issue is to explore the potential of on-chip machine learning, to reveal emerging algorithms and design needs, and to promote novel applications for learning. A holistic approach of concurrent innovations in hardware and algorithms is essential to support real-time information analytics under stringent power constraints in a mobile system.

The key topics of interest include, but are not limited to the following:

- Hardware acceleration for machine learning
- Deep learning with high speed and high power efficiency
- Hierarchical learning and classification on a chip
- Hardware implementation of sparse coding, feature extraction and personalization
- Hardware and computation models of the cortical and sensory systems
- Nanoelectronic devices, circuits and architectures for neuromorphic computing
- Emerging applications of on-chip learning, including mobile computing, automotive vision, etc.

Submit to: <http://mc.manuscriptcentral.com/jetc>

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Special Issue Timeline:

- Submission Deadline: June 30, 2018
- Author Notification: September 1, 2018
- Revised Manuscript Due: October 15, 2018
- Notification of Acceptance: December 15, 2018
- Final Manuscript Due: January 15, 2019
- Tentative Publication Date: August 2019

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