Special Issue on

Nanoelectronic Circuit and System Design Methods for Mobile Computing Era

ACM Journal on Emerging Technologies in Computing Systems (JETC)

The use of smart mobile phones, tablets, and notebooks which are different forms of mobile computing platform defines the present age social life style. Such heavy demand for ever smaller, portable, low-energy, high-performance, and secure electronic systems has been the primary driver for recent VLSI technology scaling. To continue coping with this trend, and to address new massive markets of the Internet of Things, many challenges still remain to be addressed such as high performance with energy constraints, low leakage dissipation, fast sleep and wake-up transitions, as well as reliability and security. In recent years, as the device sizes have reduced below 10nm, the challenges of design and manufacturing engineers have increased multifold. One example is leakage current, which due to continuous scaling of device geometry now represents a significant proportion of the power consumption. For example, a smartwatch battery life is consumed in a matter of 24hours only! Thus, at device-level alternative device architectures, e.g. thin film devices like FinFET or FDSOI, nanowires or 3-D transistor are introduced and proposed for the next nodes. Simultaneously alternative to Flash memory are explored and most of the proposals are based on resistive devices, e.g. MRAM, PCRAM, ReRAM. Designers have to assess the benefits of these new devices as well as to innovate by exploiting their unique capabilities. Better system level architectures are also required for high-performance at minimum energy, and reliability. Finally, circuit- and system-level solutions are needed to improve security of the information being processed by the hardware.

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Information for Authors

Information about JETC, including instructions for manuscript preparation, is available at http://jetc.acm.org. Please submit your manuscript electronically at http://mc.manuscriptcentral.com/jetc, and indicate “Special Issue on Nanoelectronic Circuit and System Design Methods for Mobile Computing Era” on the cover page and in the notes section of the submission form. Manuscripts must conform to the JETC style (double-spaced in 10-point font), and be limited to 20 pages for research papers, and 40-50 pages for tutorial and survey papers. Expanded versions of previously published conference research papers should contain at least 30% new material; authors should clearly state in a footnote on the first page how the manuscript differs from the conference paper. Papers simultaneously submitted elsewhere may be returned without review. Longer papers can be considered upon request and at the discretion of the Editor-in-Chief.

Important Dates:

- Submission Deadline: 30 September 2015
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